Please amend the claims as followed:

a1 3. (Amended) The memory element of claim 1, wherein said second region is doped differently from said first region.

a2 6. (Amended) The memory element of claim 1, wherein said conductive sidewall spacer comprises polysilicon.

a3 12. (Amended) The memory element of claim 1, wherein said conductive sidewall spacer includes at least one raised portion extending to an end adjacent to said memory material.

a4 16. (Amended) The memory element of claim 14, wherein said second region is doped differently from said first region.

a5 19. (Amended) The memory element of claim 14, wherein said conductive liner comprises polysilicon.

a6 25. (Amended) The memory element of claim 14, wherein said conductive liner includes at least one raised portion extending to an end adjacent said memory material.

Please add claims 59 to 71.

59. An electrically operated memory element, comprising:

a volume of memory material programmable to at least a first resistance state and a second resistance state; and

an electrical contact in electrical communication with said memory material, said electrical contact including at least a first region having a first resistivity and a second region having a second resistivity greater than said first resistivity.

60. The memory element of claim 59, wherein substantially all of said electrical communication is through at least a portion of an edge of said electrical contact.

61. The memory element of claim 59, wherein said electrical contact is a contact layer.

62. The memory element of claim 59, wherein said electrical contact comprises a sidewall layer.

63. The memory element of claim 59, wherein said first region is doped differently from said second region.

64. The memory element of claim 59, wherein said electrical contact comprises polysilicon .

65. The memory element of claim 61, wherein said contact layer is substantially vertically disposed.

cont. a1

66. The memory element of claim 59, wherein said electrical contact includes a raised portion extending to an end adjacent said memory material.

67. An electrically operated memory element, comprising:

a substrate;

a first dielectric layer formed over said substrate, said first dielectric layer having a sidewall surface formed therein;

a first conductive layer formed on said sidewall surface, said first conductive layer including a first region having a first resistivity and a second region having a second resistivity greater than said first resistivity;

a second dielectric layer formed over said first conductive layer wherein an edge portion of said first conductive layer is exposed, said second region being adjacent to said exposed edge portion and said first region being remote to said exposed edge portion;

a programmable resistance memory material formed over said exposed edge portion; and

a second conductive layer formed over said memory material.

68. The memory element of claim 67, wherein said first conductive layer comprises polysilicon.

69. The memory element of claim 68, wherein said polysilicon is n-type doped polysilicon or p-type doped polysilicon.

70. The memory element of claim 67, wherein said first region is doped differently from said second region.

71. The memory element of claim 67, wherein said memory material is a phase-change material.